

Integration of Circuit Design and Signal Integrity Analysis: An applied frequency-domain approach

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Abstract

In this proposal a new methodology of system-level analysis for high-speed data transfer systems is presented. The methodology integrates CMOS AFE circuits and interconnect modeling into one simulation process, based on frequency-domain analysis, which is better suited for analog signal processing. The emphasis will be made on computationally efficient simulation process that yields comprehensive system performance data.

The outcome of the project will allow avoiding deficiencies associated with time-domain simulation methodology – lengthy and labor-intensive modeling, incomplete point solutions, and often disjoint results pertaining to circuit and interconnect performance. By transforming signal specifications and system parameters into frequency domain, we will arrive to the possibility of solving for worst-case random combinations in a much more direct manner. This will allow for computationally efficient and high-confidence I/O system design.

TECHNICAL PROPOSAL

1. Problem statement

This project will focus on the development of novel methodology for high-speed signaling architecture (gigabit I/O) analysis from the system-level performance perspective. Currently, I/O interface design is complicated by numerous parameters outside of circuit designer's control: process variation, composition and structure of interconnect, power delivery noise, etc. When a full architecture is assembled, these detrimental factors are seen to significantly affect signal integrity, forcing design redo. In addition to the deterministic variations in overall system performance due to the known parameters of system components, there are also random variations, which appear only after manufacturing. Even though sub-groups that work on the separate pieces of I/O's analog front-end (AFE) – transmitter and receiver – may perform well in designing to certain signal specifications, their solutions will often result in sub-optimal functionality, or even interface failure, due to certain combinations of random parameters, such as exact transistor and package dimensions after manufacturing, and routing traces' length and topology variations over a certain range. To mitigate these concerns several strategies are currently employed industry-wide, most of which rely upon time-domain simulations of the transmitter and receiver circuits under several process-voltage-temperature (PVT) conditions and performing a separate study of interconnect from a signal integrity perspective, which commonly results in routing guidelines. Power delivery and package model analyses are also performed, usually by separate sub-groups. This kind of approach is usually very time-consuming, but, more importantly, it does not solve the issue of a disjointed design methodology that does not provide a high-confidence system-level solution space, particularly, as device sizes are moving deeper in nanoscale and switching frequencies growing to several gigabits-per-second (Gb/s). It is a problem recognized by industrial and academic communities alike – e.g. one of the preeminent goals of the Center for Circuit & Systems Solutions (C2S2), a consortium of 10 leading U.S. universities chartered by the semiconductor industry and Department of Defense, is to “Develop radical new design flows to support rapid evolution from algorithms to architectures to silicon, for complex digital and nonlinear analog/RF designs.”*

2. General method of solution

The general approach to this problem's solution is via comprehensive modeling of the system- or platform-level structure [1 – 4]. First, the decision is made as to what architecture topologies are to be included in the model – this is dictated by the application data. Second, system parameters of interest are identified – i.e. the circuits and interconnect are parameterized in terms of values known to vary as a result of manufacturing/assembly process. Then, the method of analysis – time-domain or frequency-domain – is chosen and performance benchmarks are defined; the latter are often derived from signal technical specifications (“signal spec”) at various points in the system's topology. Finally, based on the simulation method selected, the daunting task of turning parameterized system components into sensible models is performed. Since many circuit elements are inherently non-linear elements, the models defining them are often represented as functions specifically constructed to describe non-linear system behavior, e.g. – Volterra series [5]. Interconnect models are usually obtained from: a). Analytical formulas describing electrical characteristics of routing elements in terms of *RLC*-equivalent circuits – particularly

* <http://c2s2.ece.cmu.edu/research/models.php>

suitable for simple and well-known structures, such as short straight routes on FR4 substrate [6]; b). 3-D extraction of S-parameters using software tools, such as Ansoft HFSS™ or Q3D Extractor® [7], or custom-designed computational tools [8]; c). Measurement-based techniques, such as S-parameter data interpolation based on laboratory tests, or predictive modeling using previous measurements [9, 10]. Sometimes it is beneficial to create a unified interconnect model using combinatorial methods – as described, e.g., in [11]. The analysis can then be completed by introducing an optimization method aimed at improving a certain performance characteristic [12].

While the general approach described above is rigorous, it is also difficult to implement as a single process. In practice, several different groups usually work on separate pieces of this approach to take advantage of parallelizing tasks. Then, the crucial step of tying these work segments into one system-level modeling scenario is often neglected – partially due to the fact that time-domain simulations are a method of choice which, however, frequently does not work well for analog systems* [13]; and partially due to the fact that the framework for incorporating disparate models into a single system-level is often not in place. This project will address both deficiencies by building a novel, frequency-domain oriented design methodology framework.

3. Proposed solution statement and strategy

Frequency-domain analysis is suited best for analog systems. It is the preferred method of analysis for RF system due to comprehensive coverage of solution space and comparatively faster execution, since there is no need to compute convolution, or solve systems of differential equation, as required for time-domain analysis [14]. The result of the frequency-domain analysis covers the entire frequency spectrum of interest, thus making it easier to see what effects various deviations from initial system parameters may produce on overall system performance – whereas time-domain simulations provide only point-solutions, which are dependent on such factors, as e.g. input signal's bit pattern. As digital signals passing through chip's AFE are de-facto becoming ultrawideband waveforms (with bit durations around and under 100ps), it increasingly makes sense to consider them harmonic-based RF signals and re-use rich research legacy of processing such signals.

However, since most often signal's specs are given in terms of time-domain characteristics, to effectively employ frequency-domain method of analysis we will need to find a robust technique of reliably translating time-domain specs into frequency-domain solution space for entire system. Thus, this is our first goal of this project. To address it, we will study frequency composition of square-wave bit patterns and the changes it undergoes as it passes through the typical interconnect, parameterized with respect to expected variations of the component dimensions.

As a next step, we will perform an extensive study of frequency-domain methods [15] used to represent non-linear and linear components in the comprehensive I/O system topology shown in Figure 1.

* This is particularly true for wide-band analog signals and systems – time-domain simulations will only provide point solutions and take significant amounts of time if decent accuracy is desired.

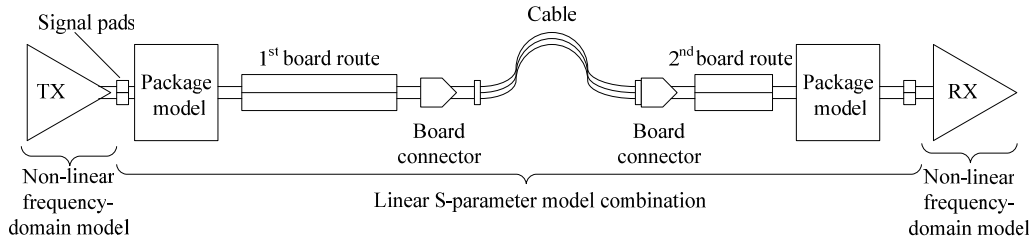


Figure 1: Full system-level I/O architecture topology

Resultant from the study will be a framework for forming a simplest possible frequency-domain simulation test-bench. Non-linear TX model components will be represented, if possible, as linear controlled source models valid for certain input frequency and voltage ranges. Linear components (on- and off-chip interconnect) will be represented with S-parameters. Some interconnect components – such as printed circuit board (PCB) traces, or cable assemblies – will have lab-measured S-parameter data associated with them. A method to efficiently inter/extrapolate S-parameters depending on components’ geometric dimensions will be developed and a solution space for all variations will be described. Resultant data will be combined into a single model, for which Z-parameters will then be derived. Then, several Thévenin’s equivalent circuits will be composed of these models.

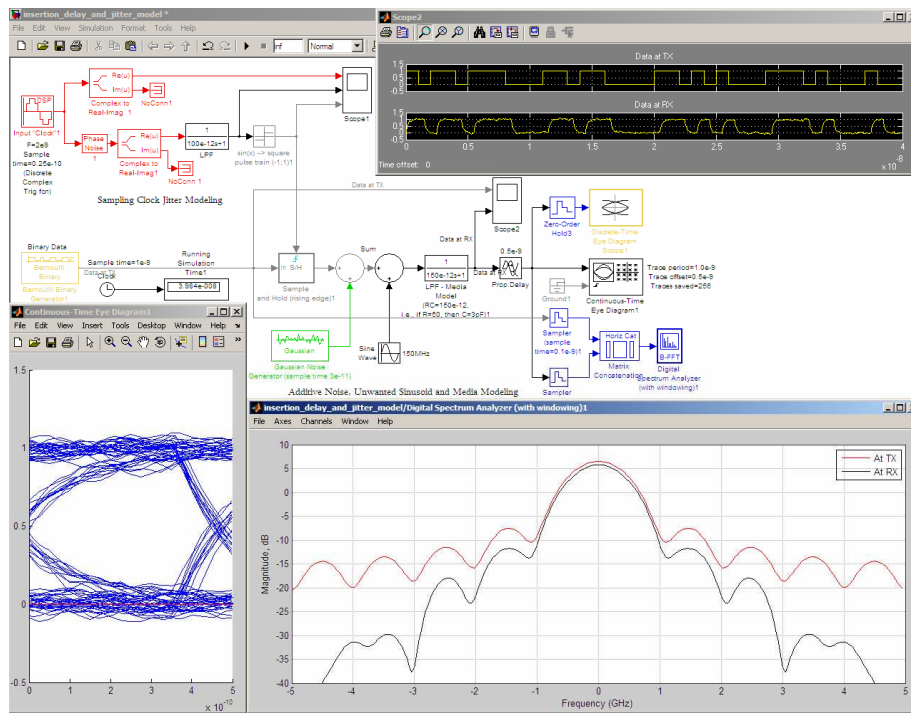


Figure 2: Simulink test-bench exploring loss and jitter effects on signal recovery in 2Gb/s system

A simple circuit incorporating Thevenin’s model of the source (valid for particular voltages and frequencies) and an equivalent model of the load will be created and simulated in frequency domain, with possible random variations being taken into account. Resultant transfer functions and reflection coefficients will then be compared to the specification bounds found earlier and high-confidence

conclusions regarding spec compliance will be presented. Post-processing step may include identification of “problem parameters” causing non-compliance.

Tools to be utilized to address these tasks are Ansoft Designer[®]/HFSS[™]/Q3D Extractor[®] – to create and verify interconnect models; Matlab[®] and Simulink[®] with RF, Communications and Signal Processing Toolboxes (Figure 2 shows Simulink implementation of a behavioral simulation of 2Gb/s data I/O with insertion loss, jitter and noise effects) – to create and verify non-linear component models, construct behavioral block-diagram based test-benches, and to perform time- to frequency-domain translation of analog signals and specs. We also expect to use Cadence[®] Virtuoso circuit design and simulation suite to verify obtained results.

4. Expected outcome and significance

The expected outcome of this project is a complete framework for frequency-domain analysis of high-speed data I/O architectures, incorporating circuit and interconnect interactions to achieve comprehensive look at overall system performance. The emphasis will be placed on computational efficiency and robust correlation of the frequency-domain optimization to time-domain signal specs. Once such a framework is established, we will provide test cases simulated both in frequency and in time domains. The system characteristics for test cases will include random variations of system components.

Primary benefit of the project’s outcome will be a *new methodology for efficient and comprehensive simulation analysis of multi-gigabit data transfer I/O systems performance*. Secondary benefits will include:

- Theoretical tool for time-domain signal spec definition into frequency domain;
- Comparative analysis of non-linear model description methods pertinent to CMOS AFE;
- Comparative analysis of optimization methods for components with random variations;
- Construction of behavioral model Simulink test-benches to simplify analyses of various system-level aspects;
- Creating a bank of Matlab routines for interconnect data processing – e.g. filter approximation based on HFSS-extracted data for particular interconnect structures to simplify and accelerate signal integrity integration.

5. Personnel and timeline

This research project will be performed by Prof. Dmitriy Garmatyuk and 2–3 undergraduate students at the Department of Electrical and Computer Engineering of Miami University. Research goals are separated into topics; each is expected to take approximately 3-6 months to complete: 1. Translation of time-domain spec into frequency-domain; 2. Quick methods of non-linear component model simulations; 3. Interconnect model extractions and combinations; 4. Thevenin (or other) multi-frequency system model creation; 5. Quick methods of obtaining performance data from resultant system-level models; 6. Compiling findings into a new frequency-domain analysis and design methodology.

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